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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/590,527	06/08/2000	Salman Akram	4101US (99-0572)	1156

7590 06/01/2005

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EXAMINER	
MITCHELL, JAMES M	
ART UNIT	**PAPER NUMBER**
2813	

DATE MAILED: 06/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/590,527	AKRAM, SALMAN	
	Examiner	Art Unit	
	James M. Mitchell	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *38-69* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *38-69* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/10/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the request for continued examination filed February 10, 2005.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claim 38-43, 48-61, 64-69 are rejected under 35 U.S.C. 102(e) as being anticipated by Potter (U.S 6,292,007).

Potter (Fig 1) discloses a semiconductor device, comprising:

(cl. 38, 53, 58, 59, 66) a substrate (101) having contact pads (102) exposed at a surface thereof, the contact pads (not labeled corresponding to pads 122 on substrate, 121) being arranged in at least one substantially linear relationship positioned proximate a centerline of the substrate and being configured to communicate with corresponding test pads (conductive material in central portion, not shown, connected to probe, 122) of a test substrate (121) upon disposing the substrate face-down over the test substrate; and at least one stabilizer (123) protruding from the surface, the at least one stabilizer being configured to at least partially stabilize an orientation of the semiconductor device upon disposal thereof face-down over the test substrate and including a plurality of

superimposed, contiguous, mutually adhered layers of the same material (i.e. material, microscopically made of multiple contiguous layers);

(Cl.39, 52, 54, 55, 67, 69) wherein stabilizer protrudes from the surface at most a distance between a plane of the surface of the substrate and a plane of a surface of the test substrate upon disposing the substrate face-down over the test substrate;

(cl. 40) when at least one conductor ("probe) connects at least one of the contact pads and a corresponding one of test pads.

(cl. 41-43, 56, 57, 64, 65) the at least one stabilizer comprises at least a semi-solid, dielectric photo polymer material (i.e. "polymer"; Col. 4, Lines 16-19).

(cl. 48) with the stabilizer stretched out in a horizontal plane and therefore elongated;

(cl. 49, 50) with the substrate comprising wafer material that is a die (i.e. "semiconductor"; Abstract);

(cl 51) the die is a chip scale package (i.e. die with exposed pads);

(cl. 60) with the contact pads in temporary communication with test pads (i.e. apparatus for testing"; Abstract);

(cl. 61) and stabilizer secured to test substrate (Fig. 1);

(cl. 68) and conductive structure (122) disposed between test substrate and semiconductor device ("DUT").

Claim 38-43, 48-61, 64-69 are rejected under 35 U.S.C. 102(e) as being anticipated by Johnson (U.S 6,469,530).

Johnson (Fig 1. 2A,B) discloses a semiconductor device, comprising:

(cl. 38, 53, 58, 59, 66) a substrate (10) having contact pads (i.e. area on chip in contact with ball, 18) exposed at a surface thereof, the contact pads (not labeled corresponding to ball, 18) being arranged in at least one substantially linear relationship positioned proximate a centerline of the substrate and being configured to communicate with corresponding test pads (area on substrate 12, in contact with ball, 18) of a test substrate (10) upon disposing the substrate face-down over the test substrate; and at least one stabilizer (28) protruding from the surface, the at least one stabilizer being configured to at least partially stabilize an orientation of the semiconductor device upon disposal thereof face-down over the test substrate and including a plurality of superimposed, contiguous, mutually adhered layers of the same material (i.e. material, microscopically made of multiple contiguous layers);

(Cl.39, 52, 54, 55, 67, 69) wherein stabilizer protrudes from the surface at most a distance between a plane of the surface of the substrate and a plane of a surface of the test substrate upon disposing the substrate face-down over the test substrate;

(cl. 40) when at least one conductor (42) connects at least one of the contact pads and a corresponding one of test pads.

(cl. 41-43, 56, 57, 64, 65) the at least one stabilizer comprises at least a semi-solid, dielectric (i.e. Functions as a standoff).

(cl. 48) with the stabilizer stretched out in a horizontal plane and therefore elongated;

(cl. 49, 50) with the substrate comprising wafer material that is a die (i.e. "IC"; Col. 1, Lines 6-10);

(cl 51) the die is a chip scale package (i.e. die with exposed pads);

(cl. 60) with the contact pads in temporary communication with test pads (i.e. apparatus for testing; Title);

(cl. 61) and stabilizer secured to test substrate (Fig. 1);

(cl. 68) and conductive structure (18) disposed between test substrate and semiconductor device (""IC").

Claim 38-43, 48-61, 64-69 are rejected under 35 U.S.C. 102(e) as being anticipated by Higgins (U.S 5,985,682).

Higgins (Fig 1, 2, 4) discloses a semiconductor device, comprising:

(cl. 38, 53, 58, 59, 66) a substrate (14) having contact pads (i.e. area on chip in contact with ball, 200) exposed at a surface thereof, the contact pads (not labeled corresponding to ball, 200) being arranged in at least one substantially linear relationship positioned proximate a centerline of the substrate and being configured to communicate with corresponding test pads (210) of a test substrate (12) upon disposing the substrate face-down over the test substrate; and at least one stabilizer (216) protruding from the surface, the at least one stabilizer being configured to at least partially stabilize an orientation of the semiconductor device upon disposal thereof face-down over the test substrate and including a plurality of superimposed, contiguous, mutually adhered layers of the same material (i.e. material, microscopically made of multiple contiguous layers);

(Cl.39, 52, 54, 55, 67, 69) wherein stabilizer protrudes from the surface at most a distance between a plane of the surface of the substrate and a plane of a surface of the test substrate upon disposing the substrate face-down over the test substrate;

(cl. 40) when at least one conductor (200) connects at least one of the contact pads and a corresponding one of test pads.

(cl. 41-43, 56, 57, 64, 65) the at least one stabilizer comprises at least a semi-solid, dielectric (i.e. Functions as a standoff).

(cl. 48) with the stabilizer stretched out in a horizontal plane and therefore elongated;

(cl. 49, 50) with the substrate comprising wafer material that is a die ("semiconductor"; Abstract);

(cl 51) the die is a chip scale package (i.e. die with exposed pads);

(cl. 60) with the contact pads in temporary communication with test pads (i.e. apparatus for testing; Title);

(cl. 61) and stabilizer secured to test substrate (Fig. 4);

(cl. 68) and conductive structure (200) disposed between test substrate (12) and semiconductor device (14).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 38-41, 44-55, 58-63 and 66-69 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art (APA) in combination with Hashimoto (US 6,410,366).

APA (FIG 1 and 2; Spec. Page 2, 3, 4 & 13) discloses an assembly, test substrate and a CSP, semiconductor device that is a die (200) comprising an inherent substrate formed from a wafer or chip scale package and contact pad (202) being arranged in at least one substantially linear relationship positioned at or proximate a centerline of said substrate and being configured to temporary communicate with corresponding test pads (230) of a test substrate (210) upon disposing said substrate face-down over said test substrate; with at least one conductive structure (220) disposed between said test substrate and said semiconductor device with said test substrate inherently in a plane (via X-axis going through middle of substrate, 214).

APA does not appear to disclose at least one elongated stabilizer protruding from said surface wherein said stabilizer is dielectric that is at least a semisolid that is comprised of a plurality of superimposed, contiguous, mutually adhered layers of the same material, said at least one stabilizer being configured to at least partially stabilize an orientation of the semiconductor device upon disposal thereof face-down over said test substrate, wherein said stabilizer protrudes from said surface at most a distance between a plane of said surface of said substrate and a plane of a surface of said test substrate upon disposing said substrate face-down over said test substrate, at least one said stabilizer positioned to be located proximate a corner of said surface and has a cross-sectional plan of an quadrilateral, or said stabilizer being secured to said surface

of said test substrate or that the stabilizer is elongated in a direction parallel to a plane in which said substrate is located.

However Hashimoto (Fig 1a-c; Col. 5, Lines 34-58) utilizes at least one elongated stabilzer comprised of the same mater via dielectric and insulating material (11, 21; Col. 5, Lines 41-44 & Col. 7, Lines 5-7) protruding from said surface wherein said stabilizer (via both portions 11 & 21) is dielectric that is at least a semisolid and that is comprised of a plurality (11, 21) of superimposed are contiguous, mutually adhered layers (Col. 4,Lines 22-26), said at least one stabilizer being configured to at least partially stabilize ("support"; i.e. prevents collapse of chip at area where stabilizers is in contact) an orientation of the semiconductor device upon disposal thereof face-down over a substrate; wherein said stabilizer protrudes from said surface at most a distance between a plane of said surface of said substrate and a plane of a surface of said substrate upon disposing said substrate face-down over substrate, and at least one said stabilizer positioned to be located proximate a corner of said surface (Fig 1A) and has a cross-sectional plan of a quadrilateral (i.e. cyclic quadrilateral); said stabilizer secured to said surface of said substrate and the stabilizer is elongated (i.e. stabilizer, 11&21, stretched along x-axis and therefore elongated) in a direction parallel to a plane in which said substrate is located (i.e. substrate in an x-axis plane).

It would have been obvious to one of ordinary skill in the art to incorporate the stabilizers of Hashimoto that are comprised of a plurality of superimposed, contiguous, mutually adhered layers with the test substrate of APA in order to provide support as taught by Hashimoto (Col. 5, Line 53).

Furthermore with respect to shape of stabilizers, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to vary the shape of the particular dimensions of the stabilizer, because applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical as supported by applicant's specification page 13 (stabilizers may be circular or alternatively rectangular or triangular), and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

Claims 42, 43, 56, 57, 64 and 65 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art (APA) and Hashimoto (US 6,410,366) as applied to claims 38, 53 and 60 and further in combination with Sasaki (JP 402210329).

Neither APA nor Hashimoto appears to disclose that the stabilizers are photopolymer, however, Sasaki (Fig 1) utilizes a photopolymer (16).

It would have been obvious to one of ordinary skill in the art to form the stabilizer of APA and Hashimoto from a photopolymer in order to provide an insulating material for the stabilizer as required by Hashimoto (Col. 5, Lines 41-44; Col. 7, Lines 5-7) and that provides uniformity of gap as taught by Sasaki (English Constitution).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James M. Mitchell whose telephone number is (571) 272-1931. The examiner can normally be reached on M-F 8:00-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jmm
April 27, 2005

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